L Number	Hits	Search Text	DB	Time stamp
1	666	CMOS and (sidewalls same (etch$3 with plasma))	USPAT; US-PGPUB	2002/03/20 15:42
2	631	(CMOS and (sidewalls same (etch$3 with plasma))) and @ad<20000518	USPAT; US-PGPUB	2002/03/20 15:42
3	160	((CMOS and (sidewalls same (etch$3 with plasma))) and @ad<20000518) and PMOS and NMOS	USPAT; US-PGPUB	2002/03/20 15:43
4	33	(((CMOS and (sidewalls same (etch$3 with plasma))) and @ad<20000518) and PMOS and NMOS) and (width with sidewalls)	USPAT; US-PGPUB	2002/03/20 15:48
5	33	((((CMOS and (sidewalls same (etch$3 with plasma))) and @ad<20000518) and PMOS and NMOS) and (width with sidewalls)) and (sidewalls with (oxide or nitride))	USPAT; US-PGPUB	2002/03/20 15:48

DOCUMENT-IDENTIFIER: US 6020231 A
TITLE: Method for forming LDD CMOS

BSPR:
A limitation with an LDD structure for a conventional CMOS device is sidewall spacer dimensions are often difficult to control as device geometry decreases. For example, the gate electrode of the conventional device is about 1 micron and below. Accordingly, the sidewall spacers include a corresponding width of about 0.2 micron and less. A conventional fabrication technique for forming such sidewall spacer is by way of CVD formation of an oxide layer, and a subsequent step of anisotropic etching, typically either reactive ion etching or plasma etching. The step of anisotropic etching is often extremely difficult to control accurately, at the smaller dimensions, thereby causing a large variation in spacer widths. The large variation in spacer widths creates devices with differing switching characteristics, which is clearly an undesirable result.

DEPR:
By way of the present thermal oxide layer, no reactive ion etch or plasma etch technique need be performed to fabricate the sidewall spacers of the conventional device. In addition, the present thermal oxide layer provides for an effective channel length of a transistor of about 0.5 microns and less and preferably about 0.35 microns and more preferably 0.25 microns and less. Of course, the dimensions used for each particular device depends upon the particular application.

	U	1 [1]	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
1	☒	☒	US 6100561 A	20000808	64	Method for forming LDD CMOS using double spacers and large-tilt-angle ion implantation	257/344	257/204 ; 257/215 ; 257/300 ; 257/327 ; 257/336 ; 257/338 ; 257/346 ; 257/351 ; 257/387 ; 257/408 ; 257/900		Wang, Chih-Hsien , et al.	☐	☐	☐	☐	☐	☐	☐
2	☒	☒	US 6020231 A	20000201	14	Method for forming LDD CMOS	438/228	438/231 ; 438/302 ; 438/595		Wang, Chih-Hsien , et al.	☐	☐	☐	☐	☐	☐	☐